Deeksha Dangwal

deekshadangwal@gmail.com | deekshadangwal | deekshadangwal.com

Research Summary

Computer architect specializing in hardware-software co-design for safe and energy-efficient systems. Pioneer in system-level privacy with "trace wringing" framework (IEEE Micro Top Pick) and novel threat models for visual feature descriptors. Created widely-used tools including PyRTL, Charm, and OpenTPU. Rising Stars in EECS recipient with 13 publications in top-tier venues (ISCA, ASPLOS, PLDI).
Most recently advancing low-power, always-on, wearable computing at Meta Reality Labs Research, enabling latency and power savings via distributed architectures and model compression.

Education

Doctor of Philosophy, Computer Science March 2022
University of California, Santa Barbara

Master of Science, Electrical and Computer Engineering September 2016
University of California, Santa Barbara

Bachelor of Engineering, Instrumentation and Electronics May 2014
M. S. Ramaiah Institute of Technology, Bangalore, India

Awards and Honors

Our paper, "SoK: Opportunities for Software-Hardware-Security Codesign for Next-Generation Secure Computing" (HASP'20) appears in the *United States National Strategy on Microelectronics Research* 2024

Runner-up, UCSB Grad Slam Competition 2021

Rising Stars in EECS, UC Berkeley 2020

IEEE Micro Top Pick, Trace Wringing for Program Trace Privacy 2020

Fiona and Michael Goodchild Graduate Mentoring Award, UCSB Graduate Division 2020

Outstanding Graduate Student Award, Department of Computer Science, UCSB 2020

Second Place, NXP Embedded Design Challenge 2015

Publications

[C]=Conference, [J]=Journal or Magazine, [W]=Workshop

[J4]: **Unlocking Visual Secrets: Inverting Features with Diffusion Priors for Image Reconstruction**
S. Q. Zhang, Z. Li, C. Guo, S. Mahloujifar, D. Dangwal, E. Suh, B. D. Salvo, C. Liu. *Transactions on Machine Learning Research **(TMLR)**, 2025*

[C6]: **Context-Aware Privacy-Optimizing Address Tracing**
D. Dangwal, Z. Zhang, J. Crandall, T. Sherwood. *IEEE International Symposium on Secure and Private Execution Environment Design **(SEED)**, 2021*

[C5]: **Porcupine: A Synthesizing Compiler for Vectorized Homomorphic Encryption**
M. Cowan, D. Dangwal, A. Alaghi, C. Trippel, V. T. Lee, B. Reagen. *Programming Language Design and Implementation **(PLDI)**, 2021*

[C4]: **Mitigating Reverse Engineering Attacks on Local Feature Descriptors**
D. Dangwal, V. T. Lee, H. J. Kim, T. Shen, M. Cowan, R. Shah, C. Trippel, B. Reagen, T. Sherwood, V. Balntas, A. Alaghi, E. Ilg. *British Machine Vision Conference **(BMVC)**, 2021*

[W3]: **SoK: Opportunities for Software-Hardware-Security Codesign for Next Generation Secure Computing**
D. Dangwal, M. Cowan, A. Alaghi, V. Lee, B. Reagen, C. Trippel. *Hardware and Architectural Support for Security and Privacy **(HASP)**, 2020*

[J3]: **Agile Hardware Development and Instrumentation with PyRTL**
D. Dangwal, G. Tzimpragos, T. Sherwood. *IEEE Micro Special Topics on Agile & Open Source Hardware, 2020*

[J2]: **Trace Wringing for Program Trace Privacy** 🏆
D. Dangwal, W. Cui, J. McMahan, T. Sherwood. *IEEE Micro's Top Picks from Computer Architecture Conferences, 2020* ***(IEEE Micro Top Pick)***
[C3]: **Safer Program Behavior Sharing through Trace Wringing** 🏆
D. Dangwal, W. Cui, J. McMahan, T. Sherwood. *Architectural Support for Programming Languages and Operating Systems* ***(ASPLOS)****, 2019*
[J1]: **Language Support for Navigating Architecture Design in Closed Form**
W. Cui, G. Tzimpragos, Y. Tao, J. McMahan, D. Dangwal, N. Tsiskaridze, G. Michelogiannakis, D. Vasudevan, T. Sherwood. *ACM Journal on Emerging Technologies in Computing Systems* ***(JETC)****, 2019*
[W2]: **PyRTLMatrix: an Object-Oriented Hardware Design Pattern for Prototyping ML Accelerators**
D. Aboye, D. Kupsh, M. Lim, J. Mai, D. Dangwal, D. Mirza, T. Sherwood. *Workshop on Energy Efficient Machine Learning and Cognitive Computing for Embedded Applications* ***(EMC2)****, 2019*
[W1]: **PyRTL in Early Undergraduate Research**
D. Mirza, D. Dangwal, T. Sherwood. *Workshop on Computer Architecture Education* ***(WCAE)****, 2019*
[C2]: **Charm: A Language for Closed-form High-level Architecture Modeling**
W. Cui, Y. Ding, D. Dangwal, A. Holmes, J. McMahan, A. JavadiAbhari, G. Tzimpragos, F. Chong, T. Sherwood. *International Symposium on Computer Architecture* ***(ISCA)****, 2018*
[C1]: **A Pythonic Approach for Rapid Hardware Prototyping and Instrumentation**
J. Clow, G. Tzimpragos, D. Dangwal, S. Guo, J. McMahan, T. Sherwood. *International Conference on Field-Programmable Logic and Applications* ***(FPL)****, 2017*

Pre-Prints, Reports, Articles

[A3]: **Unlocking Visual Secrets: Inverting Features with Diffusion Priors for Image Reconstruction**
S. Q. Zhang, Z. Li, C. Guo, S. Mahloujifar, D. Dangwal, E. Suh, B. D. Salvo, C. Liu. *arXiv preprint, December 2024*
[A2]: **Mechanism Design for Improving Hardware Security Workshop Report** *CCC Workshop Report, August 2022*
[A1]: **Analysis and Mitigations of Reverse Engineering Attacks on Local Feature Descriptors**
D. Dangwal, V. T. Lee, H. J. Kim, T. Shen, M. Cowan, R. Shah, C. Trippel, B. Reagen, T. Sherwood, V. Balntas, A. Alaghi, E. Ilg. *arXiv preprint, May 2021*

Patents

[P1]: **Deriving a concordant software neural network layer from a quantized firmware neural network layer**
J. Fowers, D. Lo, D. Dangwal *US Patent 11556764B2, Microsoft Technology Licensing LLC, 2023*

Experience

Research Scientist, *Reality Labs Research, Meta* January 2022 - April 2025

- Led innovation in energy-efficient system design for AR/smart glasses, achieving 93% latency improvements and 74% power reduction through strategic compute placement and model compression
- Invented novel low-power always-on event-based wake-up system using hand gestures on custom accelerators for optimized smart glasses interactions
- Built system-level power and performance modeling tool for Aria wearable devices using discrete-event simulation
- Developed security and privacy research program for mixed and augmented reality, establishing threat models for codec avatars, crowdsourced data collection; published in BMVC 2021, TMLR 2025 (see [C4], [J4], [A1])

Graduate Student Researcher, *ArchLab, UC Santa Barbara* June 2015 - December 2021

- Developed trace wringing framework for safer program behavior sharing, achieving privacy through extreme lossy compression with verifiable leakage bounds; published in ASPLOS 2019 (see [C3]) and recognized as IEEE Micro Top Pick (see [C6], [J2])
- Co-developed PyRTL, a Pythonic hardware development toolkit enabling rapid prototyping and agile hardware design; published in FPL 2017 (see [C1]) and IEEE Micro 2020 (see [J3])
- Worked on Charm, a domain-specific language for closed-form high-level architecture modeling; published in ISCA 2018 (see [C2])
- Led OpenTPU development in PyRTL, creating open-source tensor processing unit implementation

Research Scientist Intern, *Reality Labs Research, Meta* June 2020 - January 2021

- Implemented novel reverse engineering attack on local feature descriptors, surpassing state-of-the-art reconstruction accuracy for user image recovery
- Established first privacy threat model for computer vision feature descriptor sharing in AR systems
- Developed privacy-preserving mitigation techniques and studied effects on downstream vision system performance; published in BMVC 2021 (see [C3])

Research Intern, *Microsoft Research* June 2018 - September 2018

- Implemented parameterizable architecture-aware machine learning graph primitives for custom hardware instructions on Brainwave Neural Processing Unit
- Built tools for automatic conversion of hardware instructions to high-level graph primitives while maintaining hardware fidelity
- Designed computational experiments for neural network model accuracy verification; resulted in patent (see [P1])

Research Assistant, *Oracle Labs* June 2016 - September 2016

- Established testing environment for measuring throughput of RAPID Data Processing Unit (DPU) network, a bandwidth-optimized big data computation architecture
- Implemented network congestion tests for best and worst case traffic conditions using hardware RPC acceleration mechanisms

Teaching and Mentorship

Teaching Assistant, CS 154: Computer Architecture, UCSB Spring 2021

Teaching Assistant, Research Mentorship Program (RMP), UCSB Summer 2019

NSF ERSP Mentor, Department of Computer Science, UCSB 2018 - 2019

- Mentored team of four UCSB Computer Science sophomores on year-long research project
- Students published "PyRTLMatrix: an Object-Oriented Hardware Design Pattern for Prototyping ML Accelerators" at EMC2 workshop (see [W2])
- Awarded university-wide Fiona and Michael Goodchild Graduate Mentoring Award for excellence in mentorship

Women in STEM Mentorship Program, UCSB 10/2016 - 03/2018

Teaching Assistant, Department of Physics, UCSB 01/2015 - 06/2015

EUREKA Mentorship Program, California NanoSystems Institute, UCSB 06/2015 - 08/2015

Students Mentored

Joann Chen (2022), Manu Kondapaneni (2020), Junayed Naushad (2019), Dawit Aboye (2018-2019), Dylan Kupsh (2018-2019), Maggi Lim (2018-2019), Jacqueline Mai (2018-2019), Angela Yung (2016-2017), Saurabh Gupta (2015)

Talks and Seminars

Performance, Power, and Privacy: Codesign Strategies for Always-On Wearables,
Washington State University, Pullman June 2025

Privacy and Security in the age of Metaverse: A case for data minimization and on-device AI,
Washington State University, Everett May 2025

A System-Level Framework for Privacy
Meta, Reality Labs Research March 2021

Arizona State University, Phoenix — March 2021
Pennsylvania State University, College Station — March 2021

Professional Service and Activities

Invited Participant, CCC Future of AI Research in Industry — July 2025
Invited Participant, CCC Computing Futures Symposium — May 2025
Invited Participant, CCC Mechanism Design for Improving Hardware Security — August 2022
uArch Workshop Organizing Committee — ISCA '25, ISCA '24, MICRO '24, ISCA '23
Program Committee Member — ASPLOS '25, HPCA '25, HPCA '24 YArch '25, ISCA '24, SEED '24, YArch '23, HASP '23
External Review Committee — MICRO '24, ISCA '22, SEED '21, ASPLOS '20 (Artifact Evaluation)
Co-President, Women in Computer Science (WiCS), UCSB — 2018 - 2020
Graduate Representative for Faculty Recruitment, Department of Computer Science, UCSB — 2019 - 2020
Graduate Representative for Diversity, Department of Computer Science, UCSB — 2018 - 2019
Grace Hopper Celebration of Women — 2017, 2018, 2019
CRA-W Grad Cohort — 2017, 2018

(Last updated: July 9, 2025)